Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application.

1-3. (cancelled)

4. (previously presented) An encoder, comprising:

a state machine configured to generate a plurality of state bits, and

an interface configured to couple an input relating to one of the state bits into the state machine during a time period,

wherein the interface is configured to couple an input signal into the state machine during a second time period, and couple a complement of said one of the state bits into the state machine during the time period.

5-12. (cancelled)

13. (currently amended) An encoder, comprising:

state generation means for generating a plurality of state bits, and

interface means for coupling an input relating to one of the state bits into the state generation means during a time period,

wherein the interface means is configured to couple an input signal into the state generation means during a second time period, and ~~coupled~~ couple a complement of said one of the state bits into the state machine during the time period.

14-21. (cancelled)

22. (currently amended) A transmitter, comprising:

an encoder ~~having~~,comprising:

a state machine configured to generate a plurality of state bits, and

an interface configured to couple an input relating to one of the state bits into the state machine during a time period; and

an RF stage coupled to the encoder;

wherein the RF stage and the encoder are each an integral part of the transmitter and wherein the interface is configured to couple an input signal into the state machine during a second time period, and ~~coupled~~ couple a complement of said one of the state bits into the state machine during the time period.

23-27. (cancelled)

28. (currently amended) A transmitter, comprising:

an encoder ~~having~~,comprising:

a state machine configured to generate a plurality of stored state bits, and

an interface configured to couple an input ~~relating to~~of at least one of the plurality of stored state bits into the state machine during a time period;

an RF stage coupled to the encoder; and

a transmit control unit coupled to the encoder, the transmit control unit being configured to control the interface;

~~wherein the RF stage and the encoder are each an integral part of the transmitter~~.

29. (previously presented) The transmitter of claim 28 further comprising a preamble generator coupled to the transmit control unit.

30. (previously presented) The transmitter of claim 28 further comprising a CRC generator coupled to the transmit control unit.

31-33. (cancelled)

34. (currently amended) A transmitter, comprising:

an encoder ~~having~~,comprising:

state generation means for generating a plurality of state bits, and

interface means for coupling an input relating to one of the state bits into the state generation means during a time period; and

an RF stage coupled to the encoder;

wherein the RF stage and the encoder are each an integral part of the transmitter and wherein the interface means are configured to couple an input signal into the state generation means during a second time period, and couple a complement of said one of the state bits into the state machine during the time period.

35-39. (cancelled)

40. (currently amended) A transmitter, comprising:

an encoder ~~having,~~comprising:

state generation means for generating a plurality of stored state bits, and

interface means for coupling an input ~~relating to~~of at least one of the plurality of stored state bits into the state generation means during a time period;

an RF stage coupled to the encoder; and

transmit control means for controlling the interface means to couple the input ~~relating to~~representative of at least one of the plurality of stored state bits into the state generation means during the time period;

~~wherein the RF stage and the encoder are each an integral part of the transmitter~~.

41. (original) The transmitter of claim 40 further comprising means for generating a preamble coupled to the transmit control means.

42. (original) The transmitter of claim 40 further comprising means for generating a CRC coupled to the transmit control means.

43-44. (cancelled)

45. (previously presented) An encoder, comprising:

a state machine configured to generate a state, and

an interface configured to serially couple an input relating to a binary representation of the state into the state machine during a time period,

wherein the interface is configured to serially couple a plurality of input signals into the state machine during a second time period, and serially couple a complement of the binary representation of the state at the end of the second period into the state machine during the time period.

46-51. (cancelled)

52. (currently amended) An encoder, comprising:

state generation means for generating a state, and

interface means for serially coupling an input relating to a binary representation of the state into the state machine during a time period,

wherein the interface comprises a switch configured to serially couple ~~the~~ input signals into the state generation means during the second time period, and serially couple a complement of the binary representation of the state at the end of the second period into the state generation means during the time period.

53-57. (cancelled)

58. (currently amended) A method of generating a signal, comprising:

generating a payload as a function of a state machine output;

generating a tail as a function of a binary representation of the state machine output at the end of the payload generation, and

appending the tail to the payload,

wherein the state machine output comprises a plurality of state bits, the tail generation comprising serially feeding a complement for each of the state bits for the binary representation of the state machine output at the end of the payload generation into the state machine.

59. (previously presented) A method of generating a signal, comprising:

generating a payload as a function of a state machine output,

generating a tail as a function of a binary representation of the state machine output at the end of the payload generation, and

appending the tail to the payload,

wherein the state machine output comprises a plurality of first state bits having a most significant bit, the tail generation comprising feeding the most significant bit of the first state bits into the state machine during a first clock cycle to generate a second plurality of state bits having a most significant bit, and feeding the most significant bit of the second state bits into the state machine during a second clock cycle.

60. (original) The method of claim 59 wherein the first state bits further comprise a least significant bit, and wherein the most significant bit of the second state bits is the least significant bit of the first state bits.

61. (currently amended) A method of generating a signal, comprising:

generating a payload as function of a state machine output,

generating a tail as a function of a binary representation of the state machine output at the end of the payload generation, and

appending the tail to the payload,

wherein the state machine output comprises a plurality of first state bits having a most significant bit, the tail generation comprising feeding a complement of the most significant bit of the first state bits into the state machine during a first clock cycle to generate a ~~second~~ plurality of second state bits having a most significant bit, and feeding a complement of the most significant bit of the second state bits into the state machine during a second clock cycle.

62. (original) The method of claim 61 wherein the first state bits further comprise a least significant bit, and wherein the most significant bit of the second state bits is the least significant bit of the first state bits.

63. (New) The encoder of claim 4, wherein the interface comprises a switch.

64. (New) The encoder of claim 4, further comprising an output including a second one of the state bits.

65. (New) The encoder of claim 64, wherein the interface comprises an output, the encoder output further including the interface output.

66. (New) The encoder of claim 4, wherein the state machine comprises a 2^P-state finite state machine where P comprises an integer greater than one.

67. (New) The encoder of claim 4, wherein the state machine includes at least two delay registers configured to delay the plurality of state bits.

68. (New) The encoder of claim 67, wherein the state machine includes an adder coupled to one of the delay registers.

69. (New) The encoder of claim 13, wherein the interface means comprises a switch.

70. (New) The encoder of claim 13, further comprising an output including a second one of the state bits.

71. (New) The encoder of claim 70, wherein the interface comprises an output, the encoder output further including the interface output.

72. (New) The encoder of claim 13, wherein the state generation means comprises a 2^P-state finite state machine where P is an integer greater than one.

73. (New) The encoder of claim 13, wherein the state generation means includes at least two delay registers configured to delay the plurality of state bits.

74. (New) The encoder of claim 73, wherein the state generation means includes an adder coupled to one of the delay registers.

75. (New) The transmitter of claim 22, wherein the interface comprises a switch.

76. (New) The transmitter of claim 22, wherein the encoder further comprises an output including a second one of the state bits.

77. (New) The transmitter of claim 76, wherein the interface comprises an output, the encoder output further including the interface output.

78. (New) The transmitter of claim 22, wherein the state machine comprises a 2^P-state finite state machine where P comprises an integer greater than one.

79. (New) The transmitter of claim 22, wherein the state machine includes at least two delay registers configured to delay the plurality of state bits.

80. (New) The transmitter of claim 79, wherein the state machine includes an adder coupled to one of the delay registers.

81. (New) The transmitter of claim 34, wherein the interface means comprises a switch.

82. (New) The transmitter of claim 34, wherein the encoder further comprises an output including a second one of the state bits.

83. (New) The transmitter of claim 82, wherein the interface comprises an output, the encoder output further including the interface output.

84. (New) The transmitter of claim 34, wherein the state generation means comprises a 2^P-state finite state machine where P is an integer greater than one.

85. (New) The transmitter of claim 34, wherein the state generation means includes at least two delay registers configured to delay the plurality of state bits.

86. (New) The transmitter of claim 85, wherein the state generation means includes an adder coupled to one of the delay registers.

87. (New) The encoder of claim 45, wherein the state machine comprises a 2^P-state finite state machine where P comprises an integer greater than one.

88. (New) The encoder of claim 45, wherein the state machine includes at least two delay registers configured to generate the state.

89. (New) The encoder of claim 88, wherein the state machine includes an adder coupled to one of the delay registers.

90. (New) The encoder of claim 52, wherein the state generation means comprises a 2^P-state finite state machine where P comprises an integer greater than one.

91. (New) The encoder of claim 52, wherein the state generation means includes at least two delay registers configured to generate the state.

92. (New) The encoder of claim 91, wherein the state generation means includes an adder coupled to one of the delay registers.

93. (New) An encoder comprising:

a state machine configured to generate a plurality of state bits having a most significant bit; and

an interface configured to couple an input representative of the most significant bit into the state machine during a time period.

94. (New) The encoder of claim 93, wherein the plurality of state bits comprises a second bit different from the most significant bit, and the interface is further configured to couple a second input representative of the second bit into the state machine during a time period.

95. (New) An encoder comprising:

a state machine configured to generate at least a first plurality of state bits; and

an interface configured to couple a plurality of inputs corresponding to the first plurality of state bits into the state machine during a time period.

96. (New) The encoder of claim 95, wherein the first plurality of state bits comprises a most significant bit of a binary representation of states assumable by the state machine.